REMARKS

Applicants note with appreciation the indication of allowable subject matter by the Examiner, namely the subject matter recited in Claims 2-14. The forgoing amendment adds new Claims 16 and 17 to better appreciate Applicants contribution to the art. Now in the application are Claims 1-17 of which Claims 1, 3, and 15 are independent. The following comments address all stated grounds for rejection, and place the presently pending claims as identified above, in condition for allowance.

Rejection of Claim 1 under 35 U.S.C. § 102:

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,406,982 of Urakami, *et al.* (hereinafter "Urakami"). Applicants respectfully traverse this rejection and contend that Urakami does not anticipate Claim 1.

Applicants invention provides a method for integrating optical devices in a single growth step by utilizing a combination of selective area growth and etch (SAGE). The first device is formed between a set of oxide masked regions while a second device is formed in an adjacent planar region which does not contain oxide mask structures. By use of SAGE in which the growth between the oxide masked regions is greater than the growth in the planar region, and in which the etch rate in the area between the oxide masked regions is substantially the same as that in the planar region, the number of active quantum layers for the first device are formed between the oxide masked regions, and a different number of layers for the second device is formed in the planar region. The use of a single growth step process is a cost saving enhancement over multi-step processes.

Conventional fabrication techniques and methodologies for monolithically integrated semiconductor devices grow layers across the whole wafer, and then areas are selectively masked and etched away. This leads to abrupt transitions between structures, for example, different sections of a waveguide. Additionally, it also requires the wafer to be removed from the growth chamber in order for the mask to be made, which is separate from the growth chamber. However, even in a high grade clean room removing the wafer from the chamber and performing the external processing lithography steps to make the mask causes a substantial detrimental effect on the device. That is,

contamination and oxidation occurs at the interface (both from the processing and from environmental contamination), necessitating lengthy cleaning, despite which, it is not possible to completely restore the surface. Consequently, the remaining contamination reduces the quality of the subsequently regrown epitaxial layers to the detriment of the device because of a layer of unwanted charge, which acts to reduce the effectiveness of the interface and necessitating an increase in a driving signal.

An advantage of a monolithically integrated semiconductor device formed in accordance with the teachings of the present invention is the avoidance of such undesirable effects at interfaces of structures caused by removing the wafer from a growth station to an etching station during device fabrication. In accordance with the teachings of the present invention a monolithically integrated semiconductor device beneficially has a mask applied before the wafer enters a growth chamber and the selective area growth in the chamber is combined with an etch step in the same processing stage.

For example, in one embodiment of the present invention, selective area growth is used to produce non-uniform epitaxial semiconductor growth followed by a substantially uniform etch, such that the areas of the thicker growth are reduced in thickness and the thinner areas are etched away completely. By repeating this process it is possible to build up layers and one section of a waveguide and not in another, before overgrowing with an upper cladding. In particular, this methodology can be applied to produce an integrated laser and electro-absorption modulator (EA), in which the active layer of the laser includes quantum wells and the active layer of the EA does not. A further advantage is the layers taper between the different portions of the waveguide, rather than being an abrupt transition, which can provide an improved control of the optical mode.

Claim 1 recites a method of forming a layer in a selected area on a wafer in a single growth step. In the single growth step, the method includes, amongst other steps, the steps of, forming a mask on a substrate of the wafer defining a selective area growth region coinciding with the selected area, the selective area growth region having a growth enhancement ratio of greater than one. The Urakami reference does not anticipate Claim 1.

The Urakami reference is concerned with filling trenches by epitaxial growth. Nonetheless, Urakami does not disclose, teach or suggest forming a layer in a selected area on a wafer in a single growth step by forming a mask on a substrate of the wafer defining a selective are growth region coinciding with the selected area, and the selective area growth region having a growth enhancement ratio of greater than one.

More specifically, Urakami discloses a polishing process for flattening, since an oxide film is not formed specially as a stopper of the polishing, a stop timing of the polishing is determined by a thickness of the remaining epitaxial film on the substrate it is able to detect by an exposure of the alignment trench. That is, the epitaxial growth is conducted after the inner surface of the trench is smoothed by thermal treatment under the low pressure atmosphere (non-oxidizing and non-nitriding). In detail, the thermal treatment in the non-oxidizing or non-nitriding atmosphere and the epitaxial growth are conducted successively in the LP-CVD chamber for conducting the epitaxial growth. At that time, the mask oxide film 102 shown in Figure 8A is removed as shown in Figure 8B for preventing separation of the mask oxide film 102 in the thermal treatment. However, Urakami does not disclose, teach, or suggest that the selective area growth region (i.e. trenches 103) have a growth enhancement ratio of greater than 1.

According to the method of Claim 1, the selective area growth region has a growth enhancement ratio of greater than 1. That is, the epitaxial growth rate in the selective area growth region compared to the epitaxial growth rate in the planar region has a ratio of greater than 1. In contrast, Urakami discloses, teaches, or suggests that the ratio of the epitaxial growth rate in the trenches to the epitaxial growth rate in the planar region is unity. Hence, Urakami does not disclose each and every element of Claim 1.

For at least these reasons, Applicants respectfully contend Urakami fails to anticipate Claim 1. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 1 under 35 U.S.C. § 102(b).

Rejection of Claim 15 under 35 U.S.C. § 103(a):

Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 3,574,008 of Rice (hereinafter "Rice") in view of Urakami. Applicants

respectfully traverse this rejection and further contend that neither Urakami nor Rice, alone or in combination, teach or suggest each and every element of Claim 15.

Claim 15 recites a method of forming a layer in a selected area on a wafer in a single growth step. The method includes, amongst other steps, the step of forming a mask on a substrate of the wafer defining a selective area growth region coinciding with the selected area, the selective area growth region having a growth enhancement ratio of greater than 1. Neither Urakami nor Rice, alone or in combination, teach or suggest such a step.

Rice teaches mushroom epitaxial growth in tier type shaped holes. More specifically, Rice teaches the epitaxial growth occurs only within the geometrically defined openings in the passivating layer. As a result, the growth is uniformly defined in the openings and the subsequent lapping operation leaves semi-isolated single crystal silicon islands that can be used for a transistor or diode fabrication using standard techniques.

Nonetheless, Rice, like Urakami, does not teach or suggest the step of forming a mask on a substrate of the wafer defining a selective area growth region coinciding with the selected area and the selective area growth region having a growth enhancement ratio of greater than 1. In contrast, Rice teaches the epitaxial growth has a growth enhancement ratio of unity like the teaching in Urakami. For at least this reason, Applicants respectfully asserts the combination of Urakami in view of Rice fails to establish a *prima facie* case of obviousness with which to reject Claim 15, because neither Urakami nor Rice, alone or in combination, teach or suggest each and every step of Claim 15.

Applicants respectfully contend that neither Urakami nor Rice, alone or in combination, detract from the patentability of Claim 15. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 15 under 35 U.S.C. § 103(a).

NEW CLAIMS

New Claims 16 and 17 depend upon independent Claim 1, and therefore incorporate the patentable features of independent Claim 1. More specifically, new Claims 16 and 17

are not anticipated by nor are they rendered obvious by the cited references either alone or in combination. Additionally, each cited reference fails to disclose, teach or suggest a method for forming a layer in a selected area on a wafer in a single growth step, that includes, amongst other steps, a step of growing, after the step of etching, another layer on the wafer, as recited in new Claim 17. Likewise, each cited reference fails to disclose, teach or suggest that during the growing step, deposition species deposited on the mask migrate from the mask to adjoining unmasked areas, as recited in Claim 16. Accordingly, new Claims 16 and 17 are patentably distinct from each of the cited references either alone or in combination.

CONCLUSION

In view of the remarks set forth above, applicants contend that claims 1-17, presently pending in the application, are patentable and in condition for allowance. If the Examiner deems that there are any remaining issues, we invite the Examiner to call the undersigned at 617-227-7400.

Respectfully submitted,

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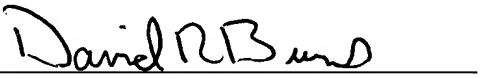

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Date: June 21, 2005